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EXAMINER
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ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/874,670	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Lex Malsawma	2825	

-- Th MAILING DATE of this communication appears on the c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22,23,28,29,34,35,40-53,58 and 59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22,23,28,29,34,35,40-49,58 and 59* is/are rejected.

7)☒ Claim(s) *50-53* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/477,865* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *9* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed March 24, 2003 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each reference listed that is not in the English language. It has been placed in the application file, but reference numbers 6 and 7 (i.e., Terada et al. and Yoshihara, T et al.) have not been considered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 22, 34, 46, and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moon (5,942,310) in view Ishizu et al. (4,984,033; hereinafter, "Ishizu").

Regarding Claim 22:

Moon discloses (in Figs. 2A-2E) a semiconductor device comprising:

a substrate 100;

at least one pixel electrode 11 formed over said substrate;

at least one TFT formed over said substrate for switching said pixel electrode, said TFT comprising:

a semiconductor layer (1, 2) having at least source, drain, and channel regions and a capacitor forming portion;

a first insulating film 5 formed on said channel region; and

a gate electrode 3 formed over said channel region with said first insulating film 5 interposed therebetween;

a storage capacitor electrically connected to said TFT, said storage capacitor comprising:

said capacitor forming portion 2 of the semiconductor layer (1, 2);

a capacitor forming electrode 4 formed over said capacitor forming portion; and

a second insulating film 6 interposed between said capacitor forming portion and said capacitor forming electrode, wherein said second insulating film 6 is thicker than said first insulating film 5.

Moon **lacks** a light shielding conductive layer formed over said substrate, wherein said light shielding film is located below the semiconductor layer. Ishizu **teaches** (in Fig. 3) it was very well known in the art to incorporate a light shielding conductive layer 2 (Col. 1, lines 56-61) and an insulating layer 3 into a device utilizing TFTs, wherein the light-shielding layer 2 is located "under" the semiconductor/active layer (4, 6). Note in Col. 1 (lines 43-55), Ishizu discloses the light-shielding layer eliminates problems associated with incident light from the outside. In summary, Moon discloses the general inventive aspect of a device comprising a TFT and a capacitor structure, wherein the TFT has an insulating film that is thicker than the insulating film of the capacitor structure; Ishizu teaches it was very well known in the art to incorporate a light shielding layer such that problems associated with incident light from the outside can be prevented by forming the light-shielding layer "under" the semiconductor/active

layer; therefore, it would have been obvious to one of ordinary skill in the art to modify Moon by incorporating a light-shielding layer (as taught by Ishizu) because the light shielding layer would effectively block incident light such that device performance would significantly improve.

Regarding Claim 34:

Moon (in view of Ishizu) discloses the claimed invention except for the specific ranges in thickness for the first and second insulating films. However, note that Moon does not specify any particular range in thickness for either the first or second insulating layer, therefore, one of ordinary skill in the art would have incorporated thickness ranges according to design needs. It would have been obvious to one of ordinary skill in the art to specify thickness ranges as currently claimed, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

Regarding Claim 46:

Ishizu discloses the light shielding conductive layer is used to block incident light entering from "outside" (Col. 1, lines 46-55), and Ishizu does not disclose that the light shielding layer is for any other purpose, i.e., there would be no apparent reason for one to increase process complexity by specifically forming an electrical connection to the light shielding layer. Therefore, it would have been obvious to one of ordinary skill in the art to specifically recite that the light shielding layer is floating.

Regarding Claim 58:

It would have been obvious to one of ordinary skill in the art to incorporate the semiconductor device of Moon (in view of Ishizu) into an electronic device selected from the list

recited in the instant claim because it was common in the art to incorporate a LCD device (similar to that disclosed Moon and Ishizu) into such electronic devices.

4. Claims 23, 35, 42, 43, 47, and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moon (5,942,310) in view Ishizu et al. (4,984,033) and Sato (5,818,552).

Regarding Claim 42:

Initially, this claim is rejected as being unpatentable over Moon (in view Ishizu) as applied to Claim 22 above, and further in view of Sato. Moon (in view of Ishizu) discloses the light shielding layer comprises chrome or the like (note Ishizu, Col. 1, lines 58-60). However, Moon (in view of Ishizu) **lacks** specifying a material from the group of materials specified in the current claim. Sato is **cited only to show** it was well known in the art that a light shielding layer can be formed of materials specified in the current claim. Sato discloses (in Fig. 2A) a light shielding conductive layer (16F, 16M) can be formed of materials including tungsten, tantalum, molybdenum, titanium, etc. (note Col. 3, lines 51-53; Col. 4, lines 20-22; and Col. 8, lines 15-21, i.e., layer "16" is specified as a black-matrix layer or a light-shielding layer). It would have been obvious to one of ordinary skill in the art to specifically form the shielding layer from a material such as those specified in the current claim because Sato shows that such materials were commonly utilized for light-shielding layers, furthermore, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding Claim 23:

Moon discloses (in Figs. 2A-2E) a semiconductor device comprising:

a substrate 100;

a semiconductor layer (1, 2) formed over said substrate, said semiconductor layer having at least a pair of impurity regions and a channel region extending therebetween and a capacitor forming portion 2 (NOTE: active semiconductor region "1" will include a pair of impurity regions and a channel region therebetween);

a "second" insulating film 5 formed on said channel region;

a "third" insulating film 6 formed on said capacitor forming portion 2 of the semiconductor layer;

a gate electrode 3 formed over said channel region;

a capacitor forming electrode 4 formed over said capacitor forming portion 2 with said "third" insulating film 6 to form a storage capacitor, wherein said "second" insulating film 5 is thicker than said "third" insulating film 6;

a "fourth" insulating film 7 formed over said storage capacitor and said gate electrode;

an electrode (8, 9) formed on said "fourth" insulating film 7;

a "fifth" insulating film 10 formed over said "fourth" insulating film 7 and said electrode; and

a pixel electrode formed on said fifth insulating film and electrically connected to one of said pair of impurity regions.

Moon **lacks** the following limitations: (1) a light shielding conductive layer over the substrate; (2) a first insulating layer formed on said light shielding conductive layer; (3) a black

mask formed on the "fifth" insulating film; and (4) a "sixth" insulating layer formed over the "fifth" insulating film and the black mask; however, it is important to note that Moon does not disclose a complete device. In regards to items "(1)" and "(2)", Ishizu **teaches** it was very well known in the art to utilize a light-shielding layer located below the semiconductor layer (see above, *Regarding Claim 22*). In regards to items "(3)" and "(4)", Sato discloses it was very well known in the art to incorporate a black matrix (i.e., a black mask) into an active matrix liquid crystal display device (AMLCD), i.e., into a device similar to that disclosed by Moon, and it was well known in the art to locate a black mask on a counter substrate or on a driving substrate (note Col. 1, lines 56-66). Sato **teaches** (in figure 1A) a device having a black mask (16M, 16P) on a driving substrate, wherein incorporating the black mask requires the following: an insulating layer 17 formed over a previously formed insulating layer 15 and over electrodes 11, 12; the black mask (16M, 16P) being formed on insulating layer 17; another insulating layer 18 formed over the black mask and the insulating layer "17"; and a pixel electrode 6 formed on the insulating layer "18". Note Sato discloses alignment precision between a pixel electrode and a black mask can be realized by incorporating the black mask into the driving substrate (note col. 1, lines 62-64). It would have been obvious to one of ordinary skill in the art to modify Moon by incorporating a light shielding layer (as taught/shown by Ishizu) and a black mask (as taught/shown by Sato) because Ishizu teaches that a light-shielding layer located under the semiconductor layer will prevent incident light from adversely affecting the device; and Sato teaches it was also well known in the art to utilize a black mask in a LCD device for shielding light (note Sato, Col. 1, lines 10-14), wherein forming a black mask as taught by Sato allows precise alignment between a pixel electrode and the black mask.

Regarding Claims 35, 43, 47, and 59:

These claims are similar to Claims 34, 42, 46, and 58 (addressed in detail above), therefore, they are held obvious over the cited references with reasoning similar to those applied to Claims 34, 42, 46, and 58.

5. Claims 28, 40, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moon (5,942,310) in view of Ishizu (4,984,033) and Misawa (5,341,012).

Regarding Claim 28:

This claim is essentially the same as Claim 22 with the exception being that it is drawn to a projector having the additional limitations of a light source. It is noted that Moon (in view of Ishizu) discloses all limitations of the liquid crystal panel (see above *Regarding Claim 22*). Misawa is **cited only** to show it was very well known in the art that a projector would include a light source in combination with an active matrix panel (i.e., a liquid crystal panel, note Fig. 18 and col. 16, lines 11-45). It would have been obvious to one of ordinary skill in the art to incorporate the semiconductor device of Moon (in view of Ishizu) into a projector having a light source because Misawa shows it was very well known in the art to make such an incorporation.

Regarding Claims 40 and 48:

These claims are similar to Claims 34 and 46 (addressed in detail above), therefore, they are held obvious over the cited references with reasoning similar to those applied to Claims 34 and 46.

6. Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moon (in view of Ishizu and Misawa) as applied to Claim 28 above, and further in view of Sato (5,818,552).

Regarding Claim 44:

This claim is similar to Claim 42 (addressed in detail above), therefore, it is held obvious over the cited references with reasoning similar to those applied to Claim 42 above.

7. Claims 29, 41, 45, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moon (5,942,310) in view of Sato (5,818,552), Ishizu (4,984,033), and Misawa (5,341,012).

Regarding Claim 29:

This claim is essentially the same as Claim 23 with the exception being that the instant claim is drawn to a projector having the additional limitations of a light source. It is noted that Moon (in view of Sato and Ishizu) discloses all limitations of the liquid crystal panel (see above *Regarding Claim 23*). Misawa is **cited only** to show it was very well known in the art that a projector would include a light source in combination with an active matrix panel (i.e., a liquid crystal panel, note Fig. 18 and col. 16, lines 11-45). It would have been obvious to one of ordinary skill in the art to incorporate the semiconductor device of Moon (in view of Sato and Ishizu) into a projector having a light source because Misawa shows it was very well known in the art to make such an incorporation.

Regarding Claims 41, 45, and 49:

These claims similar to Claims 34, 42, 46, and 58 (addressed in detail above), therefore, they are held obvious over the cited references with reasoning similar to those applied to Claims 34, 42, 46, and 58.

Allowable Subject Matter

8. Claims 50-53 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Status of the Claims

9. Claims 22, 23, 28, 29, 34, 35, 40-53, 58, and 59 are pending.

10. Claims 22, 23, 28, 29, 34, 35, 40-49, 58, and 59 are rejected.

11. Claims 50-53 contain allowable subject matter.

Remarks

12. Applicant's remarks/arguments have been fully considered, and in reference to the objections to the current disclosure, the remarks/arguments are persuasive. Accordingly, those objections have been removed. Applicant's remarks/arguments regarding the combination of references (i.e., Moon, Sato, and any secondary reference) not persuasive for the reasons provided above in the rejections under 35 USC § 103.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 703-306-5986.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 703-308-1323. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Lex Malsawma

September 16, 2003

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
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